Latent Damage due to Multiple ESD Discharges

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Abstract – ESD protection diodes are stressed with multiple discharges. We find a strong dependence of the maximum allowable number of stresses from the stress level. Ambient temperature and the pulse shape have an additional influence. Electrical characteristics are not altered til destruction. Physical failure analysis shows latent damage in the form of the gradual formation of a spike front that eventually shortens the junction.

I. Introduction

Multiple stress tests for ESD protection structures are not yet common. Practical reasons limit the number of stresses to the tens. But for critical applications in handheld equipment there might occur hundreds or even thousands of stresses during the lifetime of the device. Therefore it is interesting to measure and understand the multiple stress behavior of - at least some typical - protection structures [1] [2] [3].

II. Measurement Technique

A. Setup

ESD stress is applied with an ESD gun that yields pulses according to IEC 61000-4-2 up to 30kV. The set-up is not identical to but resembles both the 'Zwickau test' and the 'HMM test' currently under discussion (see: draft for standard practice 5.6 of the ESD Association).

Devices are assembled to a small test board. Contact discharge is used, the tip of the gun connected to the pad on the board that is connected to the pin under test of the device, the ground of the gun connected similarly. Devices are defined as failed when a major change in electrical performance is measured, like open, short, increased leakage current, reduced breakdown voltage or others.

Additional stress measurements were done with 100ns transmission line pulses (TLP).

B. Measurement Procedure

At first one sample is stressed with ten pulses at a relatively low stress level and checked afterwards electrically. If it is still okay the stress level will be increased and another ten pulses applied to the sample. This is continued until eventually the sample is defect; the last but one stress level is defined as the maximum tolerable stress level. (Obviously the same procedure could be done with a single pulse instead of ten pulses. The principle is the same and the results are comparable.) This is repeated for a certain number of samples (typically 3 to 5) and gives the maximum stress level for that device and estimation for the spread of that value. Then a stress level slightly below the maximum level is chosen and multiple stresses are applied to a fresh sample; the sample being regularly checked after several stress pulses. In that way the maximum tolerable number of stress pulses for that stress level is found. The same is repeated for other stress levels so that at the end a list of stress levels and corresponding maximum stress numbers is available. This data is plotted with the logarithm of the number of stresses on the horizontal axes and the corresponding stress level divided by the maximum stress level on the vertical axes. An exemplary graph is shown in figure 1.

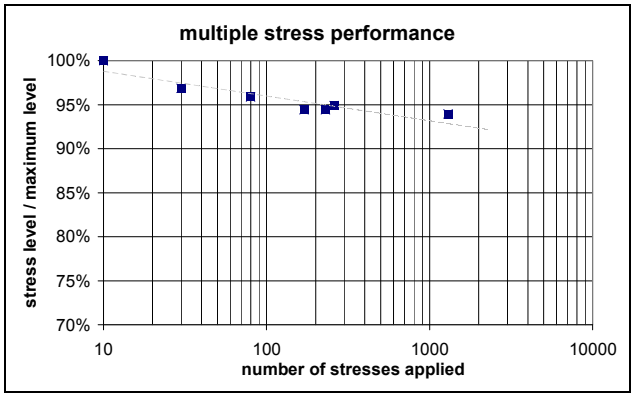

Figure 1: maximum number of stresses versus relative stress level for a reverse biased avalanche diode

Typically a logarithmic dependence is found. The slope of the curve (defined as the decrease of maximum stress level for each decade of number of stresses) can be used to characterize the device. Usually the values for the slope range from zero up to several percent.

II. Forward Diode Tested

A. Structure

Device A is a simple circular diode that is included in an on-board ESD protection device. The diode is part of a rail-to-rail set-up and is therefore stressed only in forward direction. It consists (Fig.2) of the base collector diode of a robust bipolar process with two metal layers. Metallization is aluminium, no barrier metals are used.

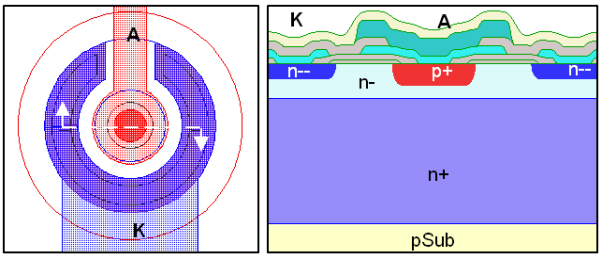

Figure 2: structure of device A

B. Multiple Stress Performance

1. Maximum Pulse Number

Device A shows a different behavior to what we have seen for other devices. The critical stress level is reduced drastically for higher numbers of pulses (Fig.3).

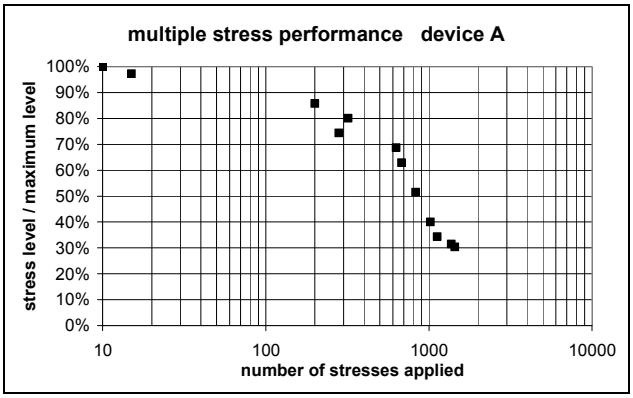

Figure 3: multiple stress performance device A

2. Sudden Death

The failure is a 'sudden death' in the sense that no degradation of the electrical performance is observed until total failure; instead stressed and unstressed samples are indistinguishable by the electrical measurements as used in this study.

E.g. the leakage current of a device that was stressed with 80% of the maximum stress level showed no increase with the number of stresses (Fig.4). Actually after the 199th stress the leakage has a normal level and only after the 200th stress the leakage increases by 5 orders of magnitude.

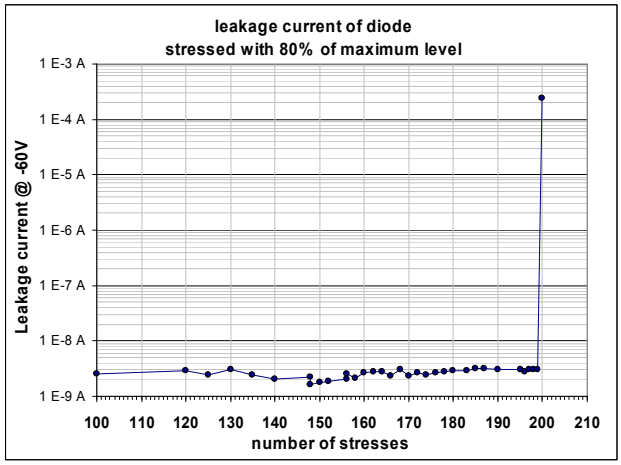

Figure 4: leakage current after multiple stresses

3. Temperature Dependence

The ambient temperature has great influence on the maximum number of pulses. When cooled the structure survives more pulses, when heated it is destroyed with less pulses (Fig.5).

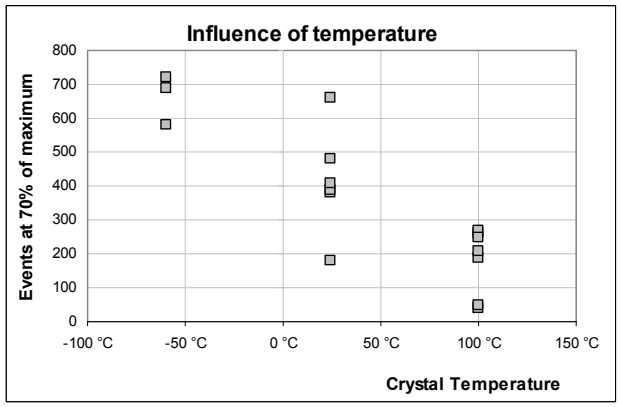

Figure 5: temperature dependence of maximum number of pulses

4. Stress under Forward Bias

Forward biasing the diode during the stress increases the maximum number of pulses (Fig.6). When strongly forward biased prior to and additional to the ESD stress the diode survives twice as many stresses as the non biased diode. Apparently the effect is limited: doubling an already high forward current (10mA to 20mA) improves the robustness of the diode only slightly.

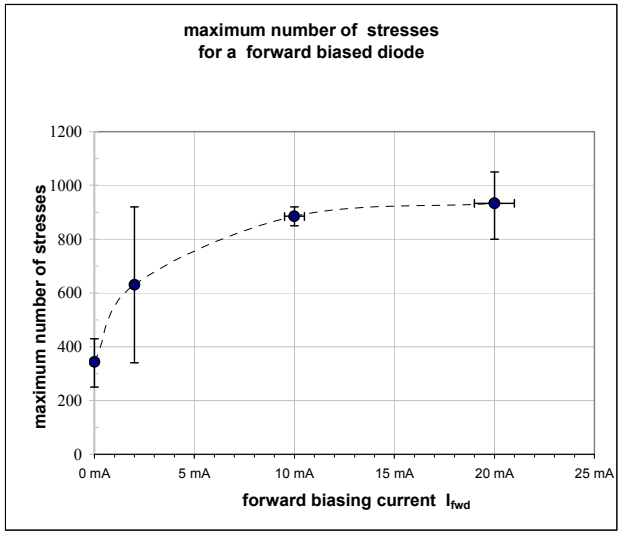

Figure 6: maximum number of stresses as a function of forward bias during stress

5. TLP Stress on Device B

TLP measurements could be done on a different but similar device: device B consists of four diodes as in device A that are connected in parallel. Device B was tested on-wafer with a commercial TLP generator (Celestron 1). Pulses with a length of 100ns and a rise time shorter than 5ns were applied. Samples of device B were stressed multiple times (up to 30.000 times) at stress levels below the maximum stress level that destroys the device within one pulse. We found a similar effect as with the ESD gun stresses of device A: a strong decrease of the tolerable stress level for higher numbers of stresses (TLP curve in fig.7).

In order to compare the effects of multiple TLP stresses with that of multiple ESD-gun stresses Device B was also tested as described in section II with ESD gun pulses according to IEC 61000-4-2. Similar to what was seen with device A the allowable stress level for device B is strongly decreased for higher numbers of stresses (ESD gun curve in fig.7).

Apparently the slope of the multiple stress curve is lower for TLP stresses than for ESD-gun stresses, e.g. at a stress level of 40% of the maximal stress level the device survives circa 600 ESD-gun stresses whilst the same device will survive more than 20.000 TLP stresses.

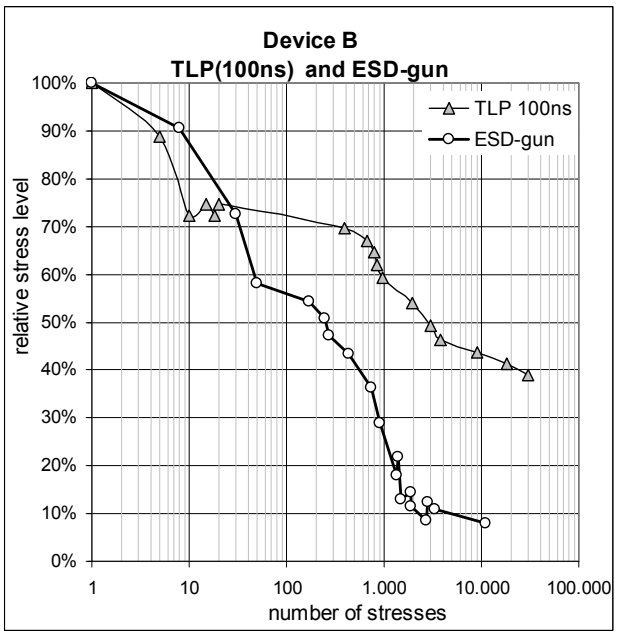

Figure 7: multiple stress performance device A: TLP and ESD-gun

C. Failure Analysis

1. LEM and OBIRCH

A sample of device A was stressed with ESD pulses until it was just defect: i.e. not yet shorted but with drastically increased leakage current. Fig.8 shows pictures of the damage position produced by LEM (light emitting microscopy) and by OBIRCH (optical beam induced resistance change).

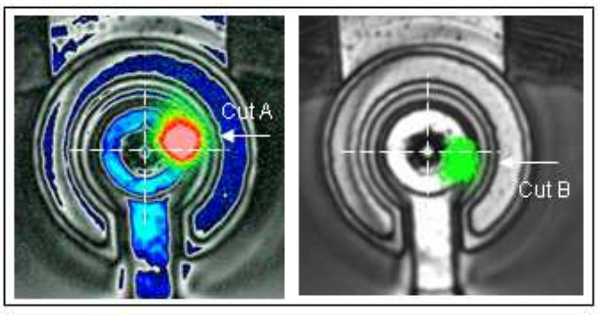

Figure 8: Damage position by LEM and by OBIRCH

Since the two failure analysis methods gave slightly different information two different cross sections were done afterwards.

2. Cross Sections

Fig.9 shows a FIB cut at position “Cut A”. Alloyed metal structures within the p+ region of the diode are visible.

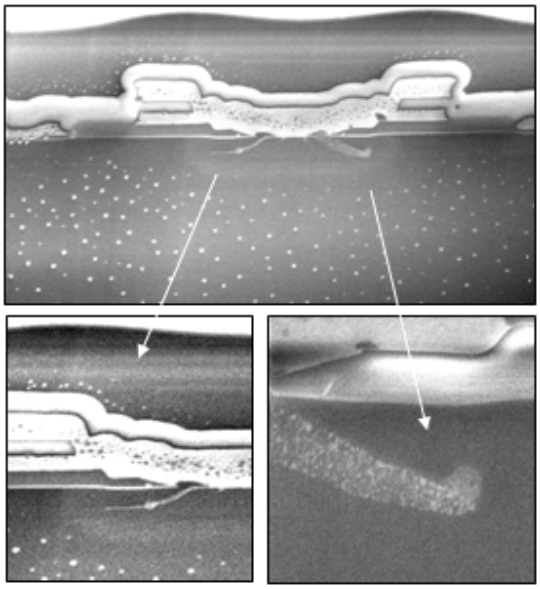

Figure 9: cross section and close-up of CUT A

At the position “CUT B” of the same sample (Fig.10) metal filaments are found that just touch the diffusion boundary p+/n. See also close-ups 1 and 2 (Fig. 11 and Fig.12).

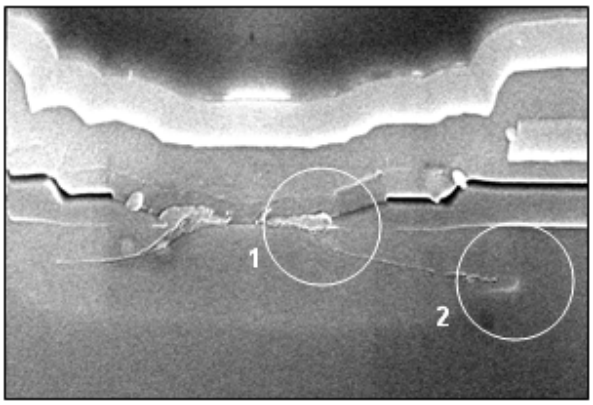

Figure 10: cross section and close-up of CUT A

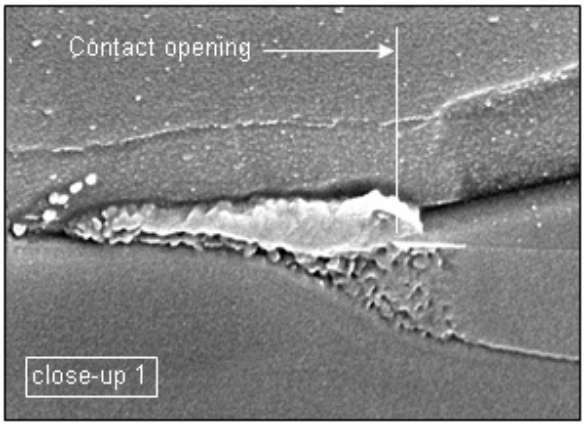

Figure 11: close-up 1 of CUT B

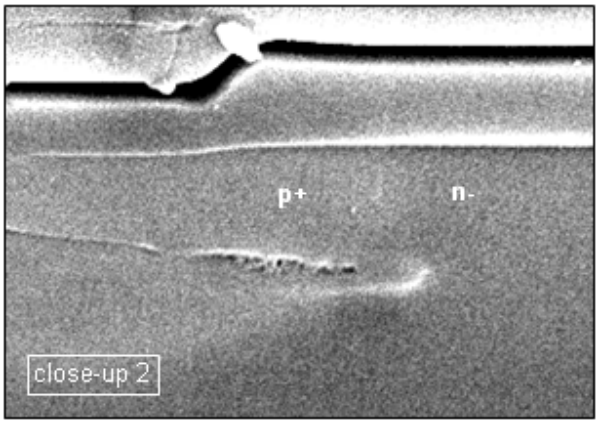

Figure 12: close-up 2 of CUT B

A different sample was stressed multiple times with a number of stresses slightly below the maximum number. The sample was still electrically okay.

The cross section (Fig.13) was selectively etched and the elemental distribution checked with EDX (energy dispersive X-ray spectroscopy).

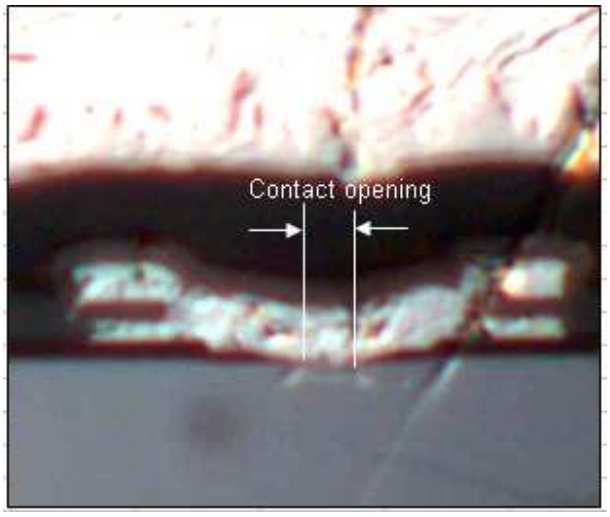

Figure 13: multiple stressed sample, electrically okay

Although the sample is electrically not yet damaged similar metal spikes can be seen as in the totally failed devices (Fig.14).

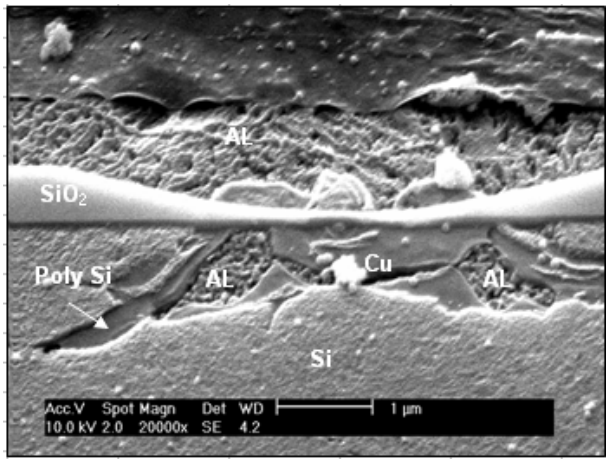

Figure 14: multiple stressed sample, electrically okay

D. Device Simulation

The spiking obviously starts at the edge of the contact opening. Device simulation actually showed that at that edge the electric field and the current density have their maximum values.

E. Discussion

The process of metal alloying starts at the edge of the contact area where current density and electric field are highest. Therefore the effect is most probably field and/or current driven. Additionally there is a temperature activated factor because higher crystal temperatures lead to faster damage.

The first peak of the ESD gun pulse has a rise time of less than 1ns. Its amplitude is rather high. The width of this first pulse is comparable to the time the diode needs to switch into a low ohmic conduction state when the bulk of the diode is flooded with charge carriers. Therefore the first peak will lead to very high electric fields within the diode and will have a disproportionately big impact on the latent damage build-up. Compared to the ESD pulse the TLP pulse rise time is slow and the diode is able to follow the rising edge of the pulse. This would explain the difference in the stress slope for the ESD-gun stress and the TLP stress.

A forward biased diode will switch faster into the low ohmic conducting mode since the charge carrier density in the diode bulk is already increased. This will decrease the disproportionate effect of the first peak and explain the positive influence of the forward biasing on the maximum number of stresses.

F. Model

Due to high current and power density at the edges of the contact opening the top metal starts to alloy at that edge into the neighbouring silicon. Most probably this effect is current and/or field driven. Each additional pulse heats the tip of the alloy front and drives it deeper into the silicon. As long as these filaments are confined within the p+ region the diode is electrically unchanged. The diode will not be measurably damaged until the filaments reach the p-n-junction. A simplified illustration of the process is shown in Fig.15.

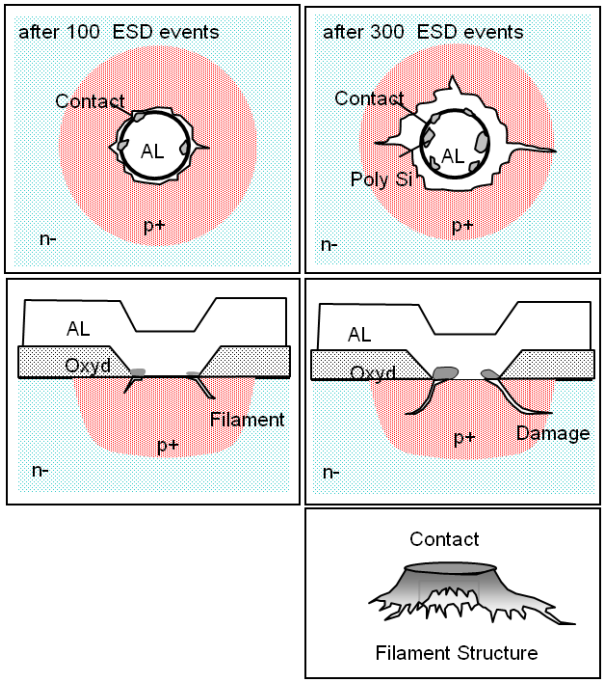

Figure 15: schematic view of ESD Degradation Phenomenon

III. Conclusion

ESD protection devices behave differently with multiple pulse stresses than with single pulses. For example the maximum allowed pulse level is usually slightly smaller for multiple pulses than for single pulses. Surprisingly a strong decrease in maximum stress level as a function of pulse number and ambient temperature is found for a bipolar forward diode. The behavior can be explained with cumulated latent damage in the form of a metal alloying front that is driven deeper with each pulse and eventually shorts the p-n-junction.

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